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09/351,544	07/12/1999	TIMOTHY K. CARNS	ZIL-204	9910

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T. LESTER WALLACE
SILICON EDGE LAW GROUP LLP
6601 KOLL CENTER PARKWAY
SUITE 245
PLEASANTON, CA 94566

EXAMINER

BROCK II, PAUL E

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 01/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/351,544	CARNS ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3-11,36-39,72-74 and 102-114 is/are pending in the application.
- 4a) Of the above claim(s) 109-114 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3-11,36-39,72-74 and 102-108 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 July 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 109 – 114 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:
2. The inventions are defined as:
 - I. Claims 3 – 11, 36 – 39, 72 – 74, and 102 – 108, drawn to a method of making a capacitor, classified in class 438, subclass 239.
 - II. Claims 109 – 114, drawn to a capacitor, classified in class 257, subclass 68.
3. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the device can be made by using the same material as the dielectric layer and the conformal insulating layer which would make the undercutting indistinguishable in the product.
4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Art Unit: 2815

5. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 109 – 114 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Drawings

6. Figures 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 102 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It

Art Unit: 2815

is not clear where in the originally filed specification support for “using isotropic wet etching” can be found.

9. Claims 107 – 108 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification support for “using isotropic etching” can be found.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 3, 8 – 11, 36, 39, 72 – 74, 102 – 105, 107, and 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (USPAT 5683931) in view of the Applicant’s admitted prior art (AAPA) and Bencher et al. (“Dielectric Antireflective coatings for DUV Lithography”, Solid State Technology, March 1997, p. 109, Bencher).

With regard to claim 3, Takahashi discloses in figures 2a – 2e forming a capacitor in an integrated circuit. Takahashi discloses in figure 2a forming a lower electrode layer (304) on a semiconductor body (301). Takahashi discloses in figure 2b forming a dielectric layer (305)

Art Unit: 2815

over a portion of the lower electrode. Takahashi discloses in figure 2b forming an upper electrode layer (306) over a portion of the dielectric layer. Takahashi discloses in figure 2c removing a portion of the upper electrode layer to expose a portion of the dielectric layer, thereby forming an upper electrode with a lateral boundary, wherein a portion of the dielectric layer is disposed in an inter-electrode region, the inter-electrode region disposed within the lateral boundary of the upper electrode and between the lower electrode layer and the upper electrode. Takahashi discloses in figure 2c subsequently removing a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode layer. Takahashi is silent to wherein a portion of the dielectric layer is removed from the inter-electrode region. Takahashi is silent to a method of etching this process step. The AAPA teaches in figure 2, figure 3, page 3, lines 11 and 12, page 4, line 25 – page 5, line 2, and page 10, lines 20 – 30 a method of etching a capacitor dielectric layer (60/160) wherein a portion of the dielectric layer is removed from an inter-electrode region (180). It would have been obvious to one of ordinary skill in the art to use the etching step resulting in removing a portion of the dielectric layer in an inter-electrode region of the AAPA in the method of Takahashi in order to perform the etching step suggested, but not defined, in column 2, lines 20 – 23, of Takahashi using a process well known as suggested by the cited sections of the AAPA. Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over a portion of the exposed portion of the lower electrode layer proximate to the portion of the dielectric layer disposed in the inter-electrode region. It would have been further obvious in the method of Takahashi and the AAPA whereby a portion of the conformal insulating layer is formed in the inter-electrode region. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to

Art Unit: 2815

forming the conformal insulating layer. Takahashi and the AAPA are silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi and the AAPA in order to improve the photolithographic process by reducing net linewidth variations as stated by the AAPA on page 1, lines 14 – 15 of the originally filed specification.

With regard to claim 8, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 9, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 10, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 11, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the plasma enhanced chemical vapor deposition anti-reflective layer (PEARL) has a thickness of 300 angstroms.

With regard to claim 36, Takahashi discloses in figure 2b forming a conductive layer on a semiconductor body. Takahashi discloses in figure 2c forming a capacitor structure comprising: a top electrode over a portion of the conductive layer, wherein the top electrode has a lateral boundary; and a dielectric layer between the top electrode and the conductive layer. Takahashi is

Art Unit: 2815

silent to a method of etching the dielectric layer. The AAPA teaches in figure 2, figure 3, page 3, lines 11 and 12, page 4, line 25 – page 5, line 2, and page 10, lines 20 – 30 a method of etching a capacitor dielectric layer (60/160) wherein a portion of the dielectric layer is removed from an inter-electrode region (180) within the lateral boundary of the top electrode and between the top electrode and the conductive layer. It would have been obvious to one of ordinary skill in the art to use the etching step resulting in removing a portion of the dielectric layer in an inter-electrode region of the AAPA in the method of Takahashi in order to perform the etching step suggested, but not defined, in column 2, lines 20 – 23, of Takahashi using a process well known as suggested by the cited sections of the AAPA. Takahashi discloses in figure 2d forming a conformal insulating layer over the capacitor structure and a portion of the conductive layer proximate to the capacitor structure, wherein a portion of the conformal insulating layer is formed in a region between the top electrode and the conductive layer. It would have been further obvious in the method of Takahashi and the AAPA whereby a portion of the conformal insulating layer is formed in the inter-electrode region within the lateral boundary of the top electrode and between the top electrode and the conductive layer. Takahashi discloses in figure 2e forming a patterned mask over the structure resultant from the forming a conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the resultant structure resultant from forming the conformal insulating layer before forming the patterned mask. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure before forming a patterned mask. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the

Art Unit: 2815

antireflective layer of Bencher on the structure resultant from the forming the conformal insulating layer and before forming the patterned mask in the method of Takahashi in order to improve the photolithographic process by reducing net linewidth variations as stated by the Applicant's admitted prior art (AAPA) on page 1, lines 14 – 15 of the originally filed specification. Takahashi discloses in figure 2e etching the conductive layer using the patterned mask.

With regard to claim 39, Takahashi discloses in figure 2e wherein the conductive layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 72, Takahashi, the AAPA, and Bencher, as combined in claim 3, teach forming a photoresist mask over a portion of the anti-reflective layer (ARL). Takahashi, the AAPA, and Bencher, as combined in claim 3, teach irradiating the photoresist with radiation that penetrates the photoresist mask. It is not clear if Takahashi and Bencher teach wherein the antireflective layer reduces a reflection of the radiation by 70% or more. The AAPA further teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces a reflection of radiation by 70% or more. It would have been obvious to use the antireflective layer of the AAPA in the method of Takahashi, the AAPA, and Bencher, as combined in claim 3, in order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6.

With regard to claim 73, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflection of the radiation by 71%.

With regard to claim 74, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a Si_xON_y film.

With regard to claim 102, as far as the examiner can ascertain, the AAPA teaches in figure 2, figure 3, page 3, lines 11 and 12, page 4, line 25 – page 5, line 2, and page 10, lines 20 – 30 wherein said subsequently removing a portion of said exposed portion of said dielectric layer in step (e) is performed using isotropic wet etching (i.e. a buffered oxide etch is an isotropic wet etch).

With regard to claim 103, Takahashi discloses in figure 2a forming a lower electrode layer (304) upon an underlying layer (302) of a semiconductor device. Takahashi discloses in figure 2b forming a capacitor dielectric layer. Takahashi discloses in figures 2b forming an upper electrode layer, wherein said capacitor dielectric layer is disposed in an inter-electrode region between said lower electrode layer and said upper electrode layer. Takahashi discloses in figure 2c removing a portion of said upper electrode layer such that an upper electrode is formed having an edge. Takahashi discloses in figure 2c removing a portion of said dielectric layer such that an exposed portion of said lower electrode layer is formed. Takahashi is silent to a method of removing the dielectric layer in such that an undercutting is formed in said inter-electrode region underneath said edge of said upper electrode, wherein said dielectric layer is absent from said undercutting. The AAPA teaches in figure 2, figure 3, page 3, lines 11 and 12, page 4, line 25 – page 5, line 2, and page 10, lines 20 – 30 removing a portion of said dielectric layer such that an exposed portion of said lower electrode layer is formed and such that an undercutting is formed in said inter-electrode region underneath said edge of said upper electrode, wherein said dielectric layer is absent from said undercutting. It would have been obvious to one of ordinary skill in the art to use the etching step resulting in removing a portion of the dielectric layer in an inter-electrode region of the AAPA in the method of Takahashi in order to perform the etching

Art Unit: 2815

step suggested, but not defined, in column 2, lines 20 – 23, of Takahashi using a process well known as suggested by the cited sections of the AAPA. Takahashi discloses in figure 2d providing a conformal insulating layer over said upper electrode and over said exposed portion of said lower electrode layer. It would have been further obvious in the method of Takahashi and the AAPA wherein providing a conformal insulating layer over said upper electrode and over said exposed portion of said lower electrode layer such that said undercutting is filled in by said conformal insulating layer. Takahashi discloses in figure 2e forming a patterned mask (309) over the structure resultant from the forming a conformal insulating layer. Takahashi is silent to providing an anti-reflective layer (ARL) over at least a portion of the resultant structure resultant from forming the conformal insulating layer before forming the patterned mask. Bencher teaches in the last paragraph before the Dielectric ARC Design section providing an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure before forming a patterned mask. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher on the structure resultant from the forming the conformal insulating layer and before forming the patterned mask in the method of Takahashi in order to improve the photolithographic process by reducing net linewidth variations as stated by the Applicant's admitted prior art (AAPA) on page 1, lines 14 – 15 of the originally filed specification. providing a anti-reflective layer over said conformal insulating layer.

With regard to claim 104, Takahashi discloses in column 2, lines 11 – 19 depositing said capacitor dielectric layer to a thickness of 400 angstroms.

Art Unit: 2815

With regard to claim 105, Takahashi discloses in column 1, line 66 wherein said underlying layer electrically isolates said lower electrode layer.

Claims 107 and 108 are rejected similar to claim 103 and 102, above.

12. Claims 4 – 7, 37, 38, and 106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi, the AAPA, and Bencher as applied to claims 3, 36, 40, 48, and 103, respectively, above, and further in view of Wang et al. (USPAT 5545585, Wang).

With regard to claim 4, Takahashi discloses in figure 2d and column 3, lines 22 – 26 wherein the conformal insulating layer is oxide. Takahashi, the AAPA, and Bencher are silent to the conformal insulating layer having a thickness in ranging from 20 angstroms to 70 angstroms. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahashi and Bencher in order to form a material of high dielectric constant that is compatible with ULSI polysilicon processing as stated by Wang in column 1, lines 16 – 17, column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 5, similar to the rejection of claim 4, above, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 6, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the thermal process is a thermal oxidation. Takahashi, Bencher and Wang do not disclose that the conformal insulating layer is formed in a rapid thermal process that is a rapid

Art Unit: 2815

thermal oxidation performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It is well known in the art to use a rapid thermal process in the production of a thermal oxide layer that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use a rapid thermal process that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C to form the conformal insulating layer of Takahashi, Bencher and Wang in order to choose a method that is widely used and understood in the art and produces a consistent and reliable oxide layer.

With regard to claim 7, similar to the rejection of claim 4, above, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is formed by deposition.

With regard to claims 37, Takahashi, the AAPA, and Bencher do not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahashi, the AAPA, and Bencher in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 38, similar to the rejection of claim 37, above, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 106, similar to claims 4 and 6 above, Takahashi, the AAPA, and Bencher in view of Wang teach wherein the providing the conformal insulating layer in step (f) is performed using a rapid thermal oxidation (RTO) process to grow a layer of silicon oxide to a thickness ranging from 20 angstroms to 100 angstroms.

Response to Arguments

13. Applicant's arguments filed November 6, 2003 have been fully considered but they are not persuasive.

14. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore, applicant's arguments are not persuasive, and the rejection is proper.

15. With regard to applicant's argument that the "cited motivation or suggestion to combine pointed to by the Examiner does not come from either Takahashi or Bencher," it should be noted that cited motivation only needs to be found in the prior art. In this case, the prior art includes the AAPA. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

16. With regard to applicant's argument that the motivation to use Bencher "is not the problem confronted by the inventors," it should be noted that if a solution to a different problem than that confronted by the applicant is solved, motivation exists for the combination. In this case, reduced linewidth variation will improve the device performance. Motivation can exist independently of the reason applicant was motivated to make the present invention. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Art Unit: 2815

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703) 308-6236. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
January 16, 2004



Tom Thomas